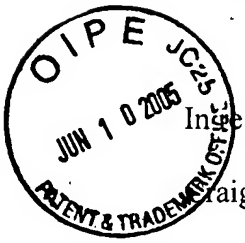
DFW

Docket No.: 043876-0145 **PATENT**



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig HANSEN, et al.	:	Confirmation Number: CNF NO. 3618
Application No.: 10/646,787	:	Group Art Unit: 2183
Filed: August 25, 2003	:	Examiner: Henry TSAI

For: PROGRAMMABLE PROCESSOR WITH GROUP FLOATING-POINT OPERATIONS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Applicants are submitting to the Office a single paper copy of each of the documents listed on the attached form PTO-1449 in connection with a corresponding Supplemental Information Disclosure Statement filing for U.S. Patent Application No. 10/418,113. Applicants are separately filing a Petition requesting waiver of Rules 1.4(b) and 98(a)(2), which requires copies of the documents listed on the attached form PTO-1449 to be provided herewith. In view of the Office's practice of scanning documents into the Image File Wrapper, it is believed that providing a single set of paper copies will enable the Office to process the papers efficiently and expedite the Examiner's consideration of the same. Furthermore, the attached form PTO-1449 includes citations

to some materials for which it is difficult to obtain additional copies. In view of the Petition and in the interests of efficiency, Applicants' respectfully request that a copy of each of the cited documents be made of record in the present application.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

In accordance with 37 CFR 1.17(p), please charge the fee of $180.00 to Deposit Account No. 500417.

Applicants bring to the Examiner's attention the following pending applications of Craig C. Hansen et al., which may include subject matter related to the present application:

Application Number	Title
10/418,113	Multiplier Array Processing System With Enhanced Utilization At Lower Precision
10/436,340	System With Wide Operand Architecture, And Method
10/616,303	Programmable Processor And Method With Wide Operations
10/705,946	Programmable Processor And Method For Partitioned Group Shift
10/712,430	System And Software For Catenated Group Shift Instruction
10/716,561	Programmable Processor And Method For Matched Aligned And Unaligned Storage Instructions
10/716,568	System And Software For Matched Aligned And Unaligned Storage Instructions
10/757,515	Method And Software For Multithreaded Processor With Partitioned Operations
10/757,516	Programmable Processor And System For Store Multiplex Operation
10/757,524	Programmable Processor And For Partitioned Group Element Selection Operation
10/757,836	Programmable Processor And System For Partitioned Floating-Point Multiply-Add Operation.

Application Number	Title
10/757,851	Method And Software For Partitioned Floating-Point Multiply-Add Operations
10/757,866	Method And Software For Store Multiplex Operation
10/757,925	Method And Software For Partitioned Group Element Selection Operation
10/757,939	Multithreaded Programmable Processor And System With Partitioned Operations

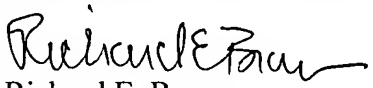
The attached form PTO-1449 includes (but is not exclusively limited to) documents that were cited in on-going litigation proceedings between the assignee of the present application, Dell Inc. and Intel Corp. (U.S. District Court for the Eastern District of Texas, Marshall Division (Civil Action No. 2:04-CV-120(TJW)). This litigation involves seven patents that are in the same family as each of the above applications.

Additionally, some documents were cited in related foreign applications. A copy of the foreign search report or office action is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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Date: June 10, 2005

OIPE JC25 JUN 10 2005 PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. **043876-0145**	SERIAL NO. **10/646,787**
	APPLICANT **HANSEN, C., et al.**	
	FILING DATE **August 25, 2003**	GROUP **2183**

EXAMINER'S INITIALS	CITE NO.	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	L-129	"IEEE Draft Standard for High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", 1995, pp.1-104, IEEE.	
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(PTO-1449)

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		EP 0 468 820 A2	01/29/1992	Fujitsu Limited			
		WO 93/01565	01/21/1993	Seiko Epson Corporation			
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		WO 97/07450	02/27/1997	Microunity Systems Engineering, Inc.			

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	L-1	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," p. 12-21, 28 March 1993, IEEE J. OF SOLID-STATE CIRCUITS.	
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	L-17	Morris A, Knapp et al.ILLIAC IV Systems Characteristics and Programming Manual (1972) "Bulk Storage Applications in the ILLIAC IV System," p. 1-10.	
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	L-51	"The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," Robert J. Gove, IEEE DSP Workshop (1994).	
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